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(54) **LOW VOLTAGE OUTPUT BUFFER AND METHOD FOR BUFFERING DIGITAL OUTPUT DATA**

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H03K 19/094 (2006.01)

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(58) **Field of Classification Search** 326/82, 326/83, 86, 87, 17, 31, 33, 56–59, 34; 327/530, 327/538, 543
See application file for complete search history.

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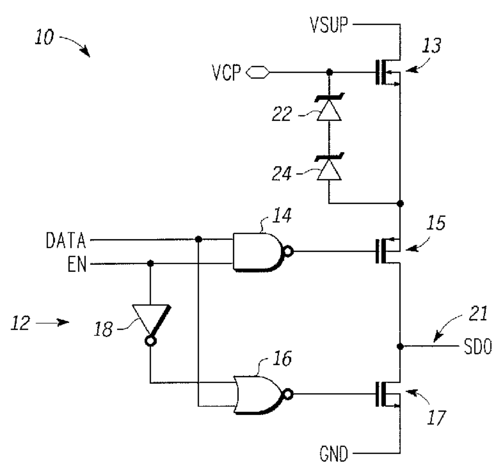
(57) **ABSTRACT**

Method and apparatus are provided for buffering a data signal to a low voltage logic device. A circuit for buffering the data signal to the low voltage logic device includes an output buffer (**12**) having first and second inputs and an output and at least one N-type isolation transistor (**13**, **19**) having a source coupled to one or both of the second input and the output. The first input receives the data signal, the second input receives a supply potential, and the output couples to the low voltage logic device. The isolation transistor has a drain for receiving a first potential and is configured to supply a second potential to the output buffer when the gate receives a bias potential. The second potential based on the first potential. The bias potential is greater than the supply potential.

9 Claims, 2 Drawing Sheets



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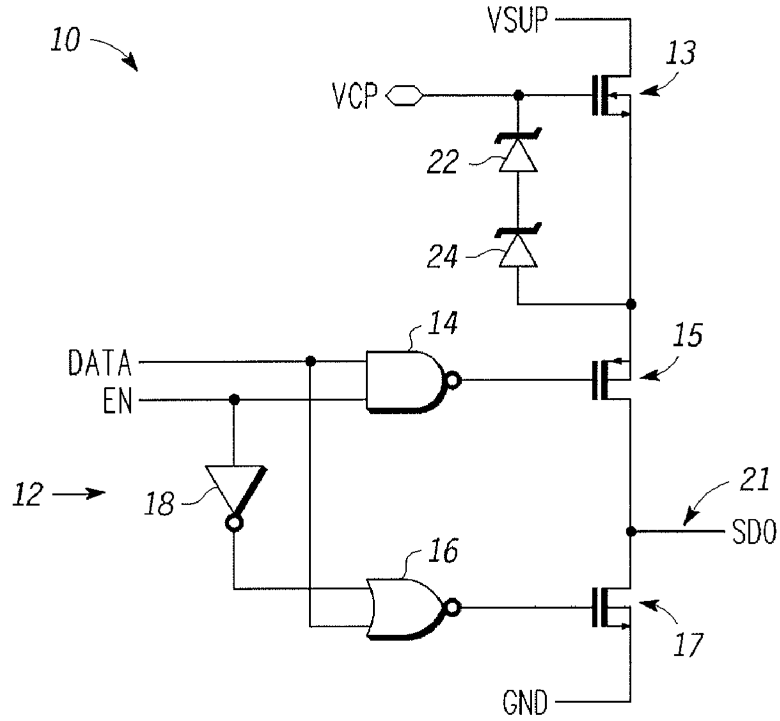
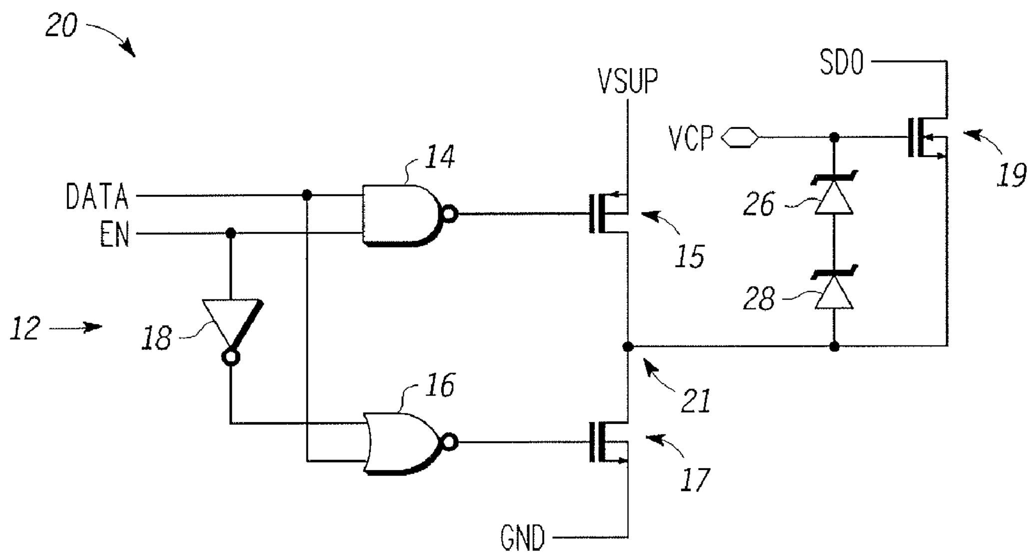

10
VSUP
13
VCP
22
24
14
15
DATA
EN
12
18
21
SDO
16
17
GND

FIG. 1


20
SDO
VSUP
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19
14
DATA
EN
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12
18
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16
17
GND

FIG. 2

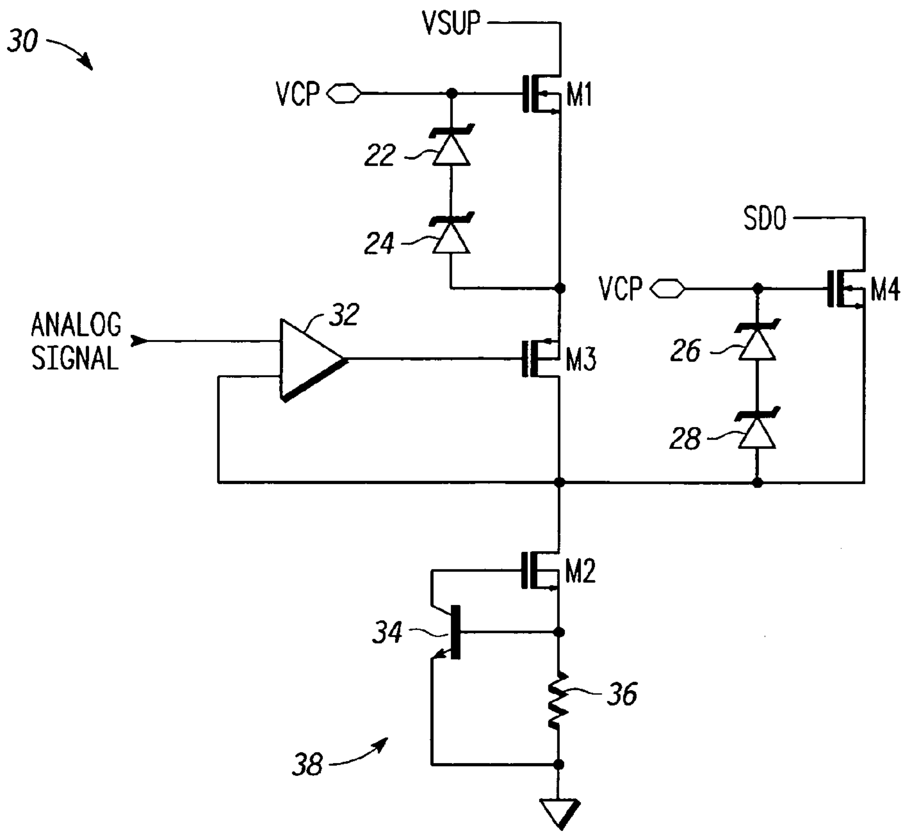
30
VSUP
VCP
M1
22
24
SDO
VCP
M4
ANALOG
SIGNAL
32
M3
26
28
M2
34
36
38

FIG. 3

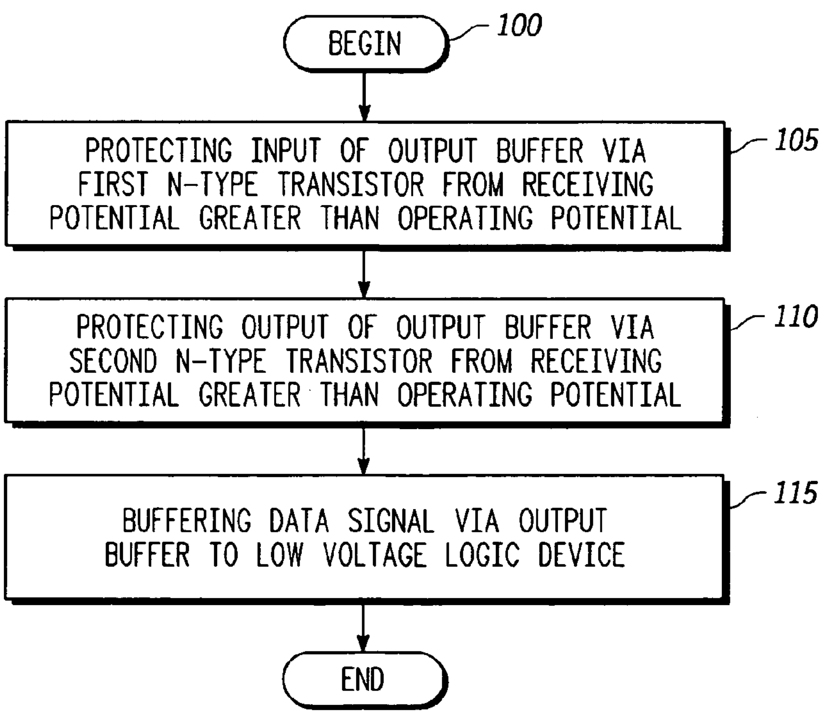
BEGIN
100
PROTECTING INPUT OF OUTPUT BUFFER VIA FIRST N-TYPE TRANSISTOR FROM RECEIVING POTENTIAL GREATER THAN OPERATING POTENTIAL
105
PROTECTING OUTPUT OF OUTPUT BUFFER VIA SECOND N-TYPE TRANSISTOR FROM RECEIVING POTENTIAL GREATER THAN OPERATING POTENTIAL
110
BUFFERING DATA SIGNAL VIA OUTPUT BUFFER TO LOW VOLTAGE LOGIC DEVICE
115
END

FIG. 4

LOW VOLTAGE OUTPUT BUFFER AND METHOD FOR BUFFERING DIGITAL OUTPUT DATA

FIELD OF THE INVENTION

The present invention generally relates to buffering data signals, and more particularly relates to circuits and methods for protecting output buffer devices.

BACKGROUND OF THE INVENTION

Logic devices (e.g., a microprocessor providing digital data) generally operate within an output voltage range between about zero volts (0V) to about five volts (5V) or less to provide logic signals, and thus the logic device has a low voltage logic to enable higher switching speeds. The logic device receives a supply voltage that is generally derived from a battery voltage, and this supply voltage is typically substantially lower than the battery voltage. In some applications (e.g., automotive applications), the battery voltage is substantially greater than the output voltage range and the supply voltage for the logic device. For example, the battery voltage may be anywhere from about twelve volts (12V) to about twenty-eight volts (28V) or even greater.

Low voltage output buffers have been used to drive digital signals to logic devices with compliance between a low signal (e.g., about zero volts (0V)) and a high signal (e.g., about 2.5 to about five volts (5V)). In these buffers, the associated transistors that gate the supply voltage to the logic device may tolerate higher voltages than the logic device. In general, however, the greater the voltage, the slower the switching speeds of the transistors. When used in an automotive application or other application with more than one power supply, a short of the output buffer to the battery voltage may affect the reliability or disable the output buffer. For example, in an integrated circuit device, the port or pin corresponding to the output logic signal may be inadvertently connected (e.g., via improper soldering or incorrect PC board trace) to a port or pin designated to provide the battery voltage. Inadvertent coupling of the inputs to the logic device or the supply voltage inputs of the output buffer to these battery voltages would likely result in a short to the higher voltage and disable the output buffer.

Accordingly, a buffer circuit is desired that prevents damage to the buffer circuit from shorts to higher voltages while having sufficiently high switching speeds. More particularly, a buffer circuit for a low voltage logic device is desired that prevents damage to the buffer circuit from shorts to higher voltages. In addition, a method for buffering a signal to a low voltage logic device is desired that prevents damage from shorts to higher voltages. Furthermore, other desirable features and characteristics of the present invention will become apparent from the subsequent detailed description of the invention and the appended claims, taken in conjunction with the accompanying drawings and this background of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will hereinafter be described in conjunction with the following drawing figures, wherein like numerals denote like elements, and

FIG. **1** is a circuit diagram of an exemplary embodiment of a supply-protected output buffer circuit in accordance with the present invention;

FIG. **2** is a circuit diagram of an exemplary embodiment of an output-protected output buffer circuit in accordance with the present invention;

FIG. **3** is a circuit diagram of another exemplary embodiment of an output buffer circuit in accordance with the present invention; and

FIG. **4** is a flow diagram of a method of communicating a data signal to a low voltage logic device in accordance with an exemplary embodiment of the present invention.

DETAILED DESCRIPTION

The following detailed description of the invention is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. Furthermore, there is no intention to be bound by any theory presented in the preceding background of the invention or the following detailed description.

The present invention is an apparatus and method for protecting the switching components of an output buffer (e.g., low-voltage high-speed transistors) from being coupled to a potential substantially greater than the proper operating range of such switching components, such as the battery voltage in a vehicle. In one exemplary embodiment, the apparatus comprises an output buffer having a supply input, a data output, and one or more isolation transistors coupled to at least one of the supply input and the data output. The output buffer is configured to couple to a low-voltage logic device at the data output. The isolation transistors are selected to have an operating range that permits biasing of such isolation transistors at a potential to prevent damage to the low-voltage high-speed transistors from shorts of the supply input and/or the data output to a battery voltage.

Referring to the drawings, FIG. **1** is a circuit diagram of an exemplary embodiment of a supply-protected output buffer circuit **10** in accordance with the present invention. The output buffer circuit **10** comprises an output buffer **12**, an isolation transistor **13**, connected to a supply input of output buffer **12**, and one or more Zener diodes **22**, **24** having a cathode coupled to a gate of isolation transistor **13** and an anode coupled to a source of isolation transistor **13**. Output buffer **12** comprises a first driver transistor **15** having a source coupled to the source of isolation transistor **13**, a second driver transistor **17** having a drain coupled to a drain of driver transistor **15**, NAND logic **14** having an output coupled to the gate of driver transistor **15**, NOR logic **16** having an output coupled to the gate of driver transistor **17**, and an inverter **18** having an output coupled to a first input of NOR logic **16**. A drain of isolation transistor **13** is configured to receive a supply potential (VSUP), and isolation transistor **13** is configured to supply this supply potential (VSUP) to the source of driver transistor **15** when a gate of isolation transistor **13** is biased at a predetermined potential. Although NAND and NOR logics **14** and **16** are paired with driver transistors **17** and **15**, a variety of logic devices and configurations of logic devices may be used with driver transistors **17** and **15**. Output buffer **12** includes first and second inputs configured to receive a data signal and an enable signal, respectively, and the drains of driver transistors **17** and **15** join to form an output **21** configured to couple with a low voltage logic device.

Output buffer **12** is a tri-state output buffer that buffers the data signal and produces an output signal (SDO) at the output **21** based on the enable signal. For example, the output signal (SDO) indicates one of a logic zero (0) or a logic one (1), corresponding with the logic indicated by the data signal, when the enable signal indicates an enabled state. The output signal (SDO) indicates no information when the enable signal indicates a non-enabled state regardless of the logic indicated by the data signal. In this exemplary embodiment, although output buffer **12** is shown as a tri-state (e.g., a current-sourcing mode, a current-sinking mode, and a floating mode) output buffer, a two-state output buffer may be used with output buffer circuit **10** that operates in two modes (e.g., current-sourcing mode and current-sinking mode). NAND logic **14** receives the data and enable signals and NANDs these signals to produce a first signal at the gate of driver transistor **15**, and NOR logic **16** receives the data signal and an inverted enable signal (e.g., via inverter **18**) and NORs these signals to produce a second signal at the gate of driver transistor **17**. The first and second signals vary between two values, a high value (e.g., a predetermined positive potential) and a low value (e.g., zero volts (0V)). The high value biases the gate of driver transistor **15** to close and biases the gate of driver transistor **17** to allow current to flow from the drain to the source of driver transistor **17**. The low value biases the gate of driver transistor **17** to close and biases the gate of driver transistor **15** to allow current to flow from the source to the drain of driver transistor **15**.

From the possible combinations of the data and enable signals supplied to output buffer **12**, three different combinations of first and second signals are produced corresponding to the three possible types of output signal (SDO) (e.g., logic zero (0), logic one (1), and no information). When the first signal is a high value and the second signal is a high value, current flows from the drain to the source of driver transistor **17** but does not flow from the source to the drain of driver transistor **15**. In this case, the potential at output **21** corresponds to zero volts (0V) based on the ground at the source of driver transistor **17** to indicate a logic zero (0). When the first signal is a low value and the second signal is a low value, current flows from the source to the drain of driver transistor **15** but does not flow from the drain to the source of driver transistor **17**. In this case, the potential at output **21** is based on the potential (VSUP) supplied to the source of driver transistor **15** to indicate a logic one (1). When the first signal is a high value and the second signal is a low value, current does not flow across driver transistors **15** and **17**. In this case, neither zero volts (0V) or the potential (VSUP) is produced at output **21** thereby indicating no information. From these types of output signals (SDO), the operating range of output buffer **12** is from about zero volts (0V) to about the potential (VSUP), and the potential (VSUP) is based on the maximum potential that may be supplied to a low-voltage logic device coupled to output **21**.

In output buffer **12**, driver transistor **17** is a positive-channel metal oxide semiconductor (PMOS) transistor and driver transistor **15** is a negative-channel metal oxide semiconductor (NMOS) transistor. Both driver transistors **17** and **15** preferably have a low voltage operating range (e.g., from about zero volts (0V) to about 3.3V or about five volts (5V)) for faster switching speeds. Isolation transistor **13** is an negative-channel metal oxide semiconductor (NMOS) transistor, and is preferably an NMOS supporting an operating range that is greater than the operating range of driver transistors **17** and **15** (e.g., from about zero volts (0V) to about ten volts (10V)). A higher operating range can be characterized by a capacity of the transistor to accept a higher potential at the gate of the transistor. NMOS transistors that are larger in size generally have higher operating ranges than smaller NMOS transistors, and thus NMOS transistors that are larger than driver transistor **17** are preferably selected for isolation transistor **13**. Additionally, other NMOS transistors, such as an N-type lateral double-diffused MOS (LDMOS) and the like, that support high voltages while having low on-resistance may be used for isolation transistor **13**. Because the operating range of isolation transistor **13** is higher than the operating range of driver transistor **17**, the switching speed of isolation transistor **13** is slower than the higher switching speed of driver transistors **17** and **15**. A voltage bias supply coupled to the gate of isolation transistor **13** biases the gate of isolation transistor **13** at a predetermined bias potential (e.g., about ten volts (10V)). Zener diodes **22** and **24** protect the gate oxide of isolation transistor **13** from transient voltages that might be present on the voltage bias supply connection, such as electrostatic discharge (ESD) pulses inadvertently applied to the voltage bias supply connection. In another exemplary embodiment, Zener diodes **22** and **24** are excluded when the bias potential from the voltage bias supply does not exceed the gate oxide breakdown voltage of isolation transistor **13**.

In operation, the gate of isolation transistor **13** is configured to receive the predetermined bias potential (e.g., a charge pumped voltage (VCP)) from the voltage bias supply. When the gate of isolation transistor **13** receives this bias potential, the potential (VSUP) is supplied to the source of driver transistor **15**. The bias potential is at least greater than the combination of the potential (VSUP) to be supplied to the source of driver transistor **15** and the threshold potential associated with isolation transistor **13**, and the bias potential is preferably sufficiently greater than this combination such that the on-resistance of isolation transistor **13** appears insignificant and minimally affects the potential at the source of isolation transistor **13**. The bias potential supplied to the gate of isolation transistor **13** is thus greater than the potential supplied to output buffer **12** at the source of driver transistor **15**. Isolation transistor **13** is selected such that the bias potential applied to the gate of isolation transistor **13** is at least greater than the combination of the potential (VSUP) and the threshold potential of isolation transistor **13**. In the event that the supply (e.g., via the drain of isolation transistor **13**) to output buffer circuit **10** is shorted to a substantially greater potential (e.g., a battery voltage) than the desired supply potential, isolation transistor **13** prevents damage to driver transistors **17** and **15** by limiting the current flowing from the drain to the source of isolation transistor **13**. For example, as the supply potential (VSUP) increases to the saturation region of isolation transistor **13**, the current flowing from the drain to the source of isolation transistor **13** substantially tapers to a maximum current. This current limiting in turn limits the potential produced at the source of isolation transistor **13**, and thus the supply potential supplied to output buffer **12** at the source of driver transistor **15**, to a value less than about the difference of the bias potential (e.g., charge pumped voltage (VCP)) and the threshold potential.

FIG. **2** is a circuit diagram of an exemplary embodiment of an output-protected output buffer circuit **20** in accordance with the present invention. Output buffer circuit **20** comprises output buffer **12**, an isolation transistor **19** having a source coupled to the output of output buffer **12**, and one or more Zener diodes **26**, **28** having a cathode coupled to a gate of isolation transistor **19** and an anode coupled to the output of output buffer **12**. Like isolation transistor **13** shown in FIG. **1**, isolation transistor **19** is an NMOS transistor, such as a high voltage lateral N-type double-diffused MOS (DMOS), and preferably supports an operating range that is greater than the operating range of driver transistors **17** and **15** (e.g., from about zero volts (0V) to about ten volts (10V)). Isolation transistor **19** is selected based on a pre-determined maximum potential produced at output **21** and thus supplied to the source of isolation transistor **19**. In this exemplary embodiment, the maximum potential produced at output **21** is the potential (VSUP) corresponding to a logic one (1) signal, and isolation transistor **19** is selected such that the bias potential applied to the gate of isolation transistor **19** is at least greater than the combination of the potential (VSUP) and the threshold potential of isolation transistor **19**. Zener diodes **26** and **28** protect the gate oxide of isolation transistor **19** from transient voltages that might be present on the voltage bias supply connection to isolation transistor **19**. Zener diodes **26** and **28** are excluded when the bias potential from the voltage bias supply does not exceed the gate oxide breakdown voltage of isolation transistor **19**.

In operation, a drain of isolation transistor **19** is configured to couple to the low voltage logic device to provide the output signal (SDO), and the gate of isolation transistor **19** is configured to receive the predetermined bias potential. In this exemplary embodiment, the bias potential of the gate of isolation transistor **19** is greater than the combination of the potential (VSUP) and the threshold potential, and the bias potential is preferably sufficiently greater than this combination such that the on-resistance of isolation transistor **19** appears insignificant and minimally affects the potential at the source of isolation transistor **19**. The potential received at the gate of isolation transistor **19** is thus greater than the potential (VSUP) supplied to output buffer **12** via the source of driver transistor **15**. In the event that the output **21** of output buffer **12** is shorted (e.g., via the drain of isolation transistor **19**) to a substantially greater potential (e.g., a battery voltage) than the desired supply potential, isolation transistor **19** prevents damage to driver transistors **17** and **15** by limiting the current flowing from the drain to the source of isolation transistor **19**. For example, as the potential produced at the drain of isolation transistor **19** increases to the saturation region of isolation transistor **19**, the current flowing from the drain to the source of isolation transistor **13** substantially tapers to a maximum current. This current limiting in turn limits the potential produced at the source of isolation transistor **19**, and thus the potential that may appear at the output **21** of output buffer **12**, to a value that is less than about the difference of the bias potential and the threshold potential of isolation transistor **19**.

FIG. **3** is a circuit diagram of another exemplary embodiment of an output buffer circuit **30** in accordance with the present invention. Although FIGS. **1** and **2** show output buffer **12** with digital logic inputs (e.g., NAND logic **14** and NOR logic **16**), analog versions of the digital logic inputs may be used with output buffer circuit **30**. Additionally, although FIGS. **1** and **2** show the individual incorporation of isolation transistors **13** and **19**, respectively, with output buffer **12**, isolation transistors **13** and **19** may be incorporated together into output buffer circuit **30**. In this exemplary embodiment, output buffer circuit **30** comprises driver transistors **17** and **15**, an operational amplifier (OPAMP) **32** coupled to driver transistors **17** and **15**, and isolation transistors **13** and **19**. Additionally, a current limiter **38** is coupled to driver transistor **17** for regulating the current at the source of driver transistor **17**. Although current limiter **38** is incorporated into output buffer circuit **30**, other circuits for regulating current at the source of driver transistor **17** may be substituted in place of current limiter **38**, such as a current detector and the like. OPAMP **32** and driver transistors **17** and **15** together form an output buffer **23** for analog signals. Isolation transistor **13** is coupled to a supply input (e.g., the source of driver transistor **15**) of output buffer **23** to limit the potential produced at the source of isolation transistor **13** and thus the supply potential supplied to output buffer **23** at the source of driver transistor **15**. The supply potential supplied to output buffer **23** is limited to a value less than about the difference of the bias potential (e.g., charge pumped voltage (VCP)) and the threshold potential. Isolation transistor **19** is coupled to an output **21** (e.g., the drains of driver transistors **17** and **15**) of output buffer **23** to limit the potential produced at the source of isolation transistor **19** (e.g., from a short of the output **21** via the drain of isolation transistor **19**) and thus the potential that may appear at output **21** of output buffer **12**. The potential that may appear at output **21** is limited to a value that is less than about the difference of the bias potential and the threshold potential of isolation transistor **19**.

In this exemplary embodiment, OPAMP **32** has a first input configured to receive an analog input signal, a second input coupled to the drains of both driver transistors **17** and **15**, and an output coupled to the gate of driver transistor **15**. Current limiter **38** comprises a transistor **34** having a collector coupled to the gate of driver transistor **17** and a resistor **36** having a first terminal coupled to a base of transistor **34** and a second terminal coupled to an emitter of transistor **34**. The base of transistor **34** is also coupled to the source of driver transistor **17**, and the emitter of transistor **34** is coupled to a reference potential (e.g., ground).

FIG. **4** is a flow diagram of a method **100** of communicating a data signal to a low voltage logic device in accordance with an exemplary embodiment of the present invention. The data signal is buffered via the output buffer to the low voltage logic device at step **115**. An input (e.g., voltage supply) of the output buffer is protected via a first N-type transistor from receiving a potential greater than an operating potential (e.g., a maximum operating potential) of the output buffer at step **105**. The gate of the first N-type transistor is biased at a potential that is greater than the operating potential. The first N-type transistor produces, at the input of the output buffer, a supply potential less than or equal to about the operating potential when the drain of the first N-type transistor receives the first potential (e.g., when the supply pin is coupled to a battery). An output of the output buffer is protected via a second N-type transistor from receiving a second potential greater than the operating potential at step **110**. The gate of the second N-type transistor is biased at a potential greater than the operating potential. The second N-type transistor produces, at the output of the output buffer, a potential less than or equal to about the operating potential when the drain of the second N-type transistor receives the second potential (e.g., when the output pin is coupled to a battery). Although the method **100** is described as both protecting the input of the output buffer and protecting the output of the output buffer, the input of the output buffer may solely be protected or the output of the output buffer may solely be protected. In one exemplary embodiment, while buffering the data signal, a supply potential is provided via an isolation transistor to the output buffer at step **110**. The gate of the isolation transistor is biased at a first potential that is at least greater than a combination of the potential at the source of the isolation transistor and a threshold potential (e.g., the threshold potential of the diodes **22** and **24** between the gate and source of the isolation transistor **13**). When biasing the gate of the isolation transistor, the first potential is selected to minimize an operating or "on" resistance of the first transistor. In another exemplary embodiment, while buffering the data signal, an output signal is transmitted via an isolation transistor at the output of the output buffer to the low voltage logic device at step **115**. The gate of the second transistor is biased at a second potential at least greater than a combination of the potential at the source of the second transistor and the threshold potential (e.g., the threshold potential of the diodes **26** and **28** between the gate and source of the isolation transistor **19**). When biasing the gate of the second transistor, the second potential is selected to minimize an operating or "on" resistance of the second transistor. In another exemplary embodiment, steps **110** and **115** are performed together while buffering the data signal. For example, the supply potential is provided via a first isolation transistor to the output buffer and the output signal is transmitted via a second isolation transistor at the output of the output buffer to the low voltage logic device while buffering the data signal.

In an exemplary embodiment, a circuit for buffering a data signal to a low voltage logic device is provided comprising an output buffer having a first input, a voltage input and an output, and a first N-type transistor having a source coupled to the second input. The first input is configured to receive the data signal, the voltage input is configured to receive a supply potential, and the output is configured to couple to the low voltage logic device. The first transistor has a drain configured to receive a first potential and is configured to supply a second potential to the output buffer when the gate receives a bias potential. The second potential is based on the first potential, and the bias potential is greater than the supply potential. The first transistor is configured to protect the output buffer at the voltage input when the second potential is greater than the supply potential. When the drain receives the first potential greater than the supply potential, the first transistor limits the second potential to the supply potential. The circuit may further comprise at least one diode having a cathode coupled to the gate and having an anode coupled to the source. The first transistor is a high voltage lateral N-type double-diffused metal oxide semiconductor. In one exemplary embodiment, the output buffer comprises second and third transistors, a NAND gate, and a NOR gate. The second transistor has a source coupled to the source of the first transistor, a drain, and a gate configured to receive a first signal. The NAND gate has an input configured to receive the data signal and has an output coupled to the gate of the second transistor. The NAND gate is configured to NAND the data signal to produce the first signal. The third transistor has a drain coupled to the drain of the second transistor forming the output of the output buffer, a source configured to couple to a third potential, and a gate configured to receive a second signal. The NOR gate has an input configured to receive the data signal and has an output coupled to the gate of the third transistor. The NOR gate is configured to NOR the data signal to produce the second signal. The second and third transistors have an operating range, and the maximum potential is based on the operating range. In another exemplary embodiment, the output buffer may comprise second, third, and fourth transistors, and a resistor. The second transistor has a source coupled to the source of the first transistor, a drain, and a gate configured to receive a first signal. The third transistor has a drain coupled to the drain of the second transistor forming the output of the output buffer, a source, and a gate configured to receive a second signal. The fourth transistor has a collector coupled to the gate of the third transistor, a base coupled to the source of the third transistor, and an emitter configured to couple to the third potential. The resistor has a first terminal coupled to the base of the fourth transistor and has a second terminal coupled to the emitter of the fourth transistor and configured to couple to the third potential. In another exemplary embodiment, the output buffer comprises second and third transistors and an operational amplifier. The second transistor has a source coupled to the source of the first transistor, a drain, and a gate. The third transistor has a drain coupled to the drain of the second transistor, a source configured to couple to a third potential, and a gate. The operational amplifier has a first input configured to receive the data signal, a second input coupled to the drain of the third transistor, and an output coupled to the gate of the second transistor.

In another exemplary embodiment, a circuit for buffering a data signal to a low voltage logic device is provided comprising an output buffer having an input and an output and a first N-type transistor having a source coupled to the output. The input is configured to receive the data signal. The output buffer is configured to produce an output signal based on the data signal, and the output signal has a maximum potential. The first transistor has a drain configured to couple to the low voltage logic device and has a gate configured to receive a bias potential. The bias potential is greater than the maximum potential. The first transistor is configured to protect the output buffer at the output when the drain receives a potential greater than the maximum potential. When the drain receives a potential greater than the maximum potential, the first transistor produces an output potential at the source that is equal to or less than the maximum potential. The circuit may further comprise at least one diode having a cathode coupled to the gate and having an anode coupled to the source. In one exemplary embodiment, the output buffer comprises second and third transistors, a NAND gate, and NOR gate. The second transistor has a source configured to couple to a first potential, a drain coupled to the source of the first transistor, and a gate configured to receive a first signal. The NAND gate has an input configured to receive the data signal and has an output coupled to the gate of the second transistor. The NAND gate is configured to NAND the data signal to produce the first signal. The third transistor has a drain coupled to the drain of the second transistor to form the output of the output buffer, a source configured to couple to a second potential, and a gate configured to receive a second signal. The NOR gate has an input configured to receive the data signal and has an output coupled to the gate of the third transistor. The NOR gate is configured to NOR the data signal to produce the second signal. The second and third transistors have an operating range, and the maximum potential is based on the operating range. In another exemplary embodiment, the output buffer comprises second, third, and fourth transistors, and a resistor. The second transistor has a source configured to couple to a first potential, a drain coupled to the source of the first transistor, and a gate configured to receive a first signal. The third transistor has a drain coupled to the drain of the second transistor and the source of the first transistor, a source, and a gate. The fourth transistor has a collector coupled to the gate of the third transistor, a base coupled to the source of the third transistor, and an emitter configured to couple to a second potential. The resistor has a first terminal coupled to the base of the fourth transistor and the source of the third transistor and has a second terminal coupled to the emitter of the fourth transistor and configured to couple to the second potential. In another exemplary embodiment, the output buffer comprises second and third transistors and an operational amplifier. The second transistor has a source configured to coupled to a first potential, a drain coupled to the source of the first transistor, and a gate. The third transistor has a drain coupled to the drain of the second transistor and the source of the first transistor, a source configured to couple to a second potential, and a gate. The operational amplifier has a first input configured to receive the data signal, a second input coupled to the drain of the third transistor, and an output coupled to the gate of the second transistor.

In another exemplary embodiment, a method for communicating a data signal from an output buffer to a low voltage logic device is provided comprising the steps of at least one of protecting an input of the output buffer via a first N-type transistor from receiving a first potential greater than an operating potential of the output buffer and protecting an output of the output buffer via a second N-type transistor from receiving a second potential greater than the operating potential, and buffering the data signal via the output buffer to the low voltage logic device. The step of protecting the input comprises biasing the gate of the first N-type transistor at a third potential greater than the operating potential. The first N-type transistor produces at the input a fourth potential less than or equal to about the operating potential when the drain of the first N-type transistor receive the first potential greater than the operating potential. The step of protecting the output comprises biasing the gate of the second N-type transistor at a third potential greater than the operating potential. The second N-type transistor produces at the output a fourth potential less than or equal to about the operating potential when the drain of the second N-type transistor receives the second potential greater than the operating potential.

While at least one exemplary embodiment has been presented in the foregoing detailed description, it should be appreciated that a vast number of variations exist. It should also be appreciated that the exemplary embodiment or exemplary embodiments are only examples, and are not intended to limit the scope, applicability, or configuration of the invention in any way. Rather, the foregoing detailed description will provide those skilled in the art with a convenient road map for implementing the exemplary embodiment or exemplary embodiments. It should be understood that various changes can be made in the function and arrangement of elements without departing from the scope of the invention as set forth in the appended claims and the legal equivalents thereof.

What is claimed is:

1. A circuit for buffering a data signal to a low voltage logic device, the circuit comprising:

a tri-state output buffer responsive to an enable signal and having at least one driver transistor having a first operating range, a first input configured to receive the data signal, a second input configured to receive the enable signal, a voltage input configured to receive a first supply potential, and an output configured to couple to the low voltage logic device, wherein the at least one driver transistor includes a first driver transistor coupled between the voltage input and the output, wherein the tri-state output buffer is adapted to provide a potential at the output that corresponds to the first supply potential when the first driver transistor is on; and

a supply-input protection circuit connected to the voltage input of the tri-state buffer and configured to provide the first supply potential, the supply-input protection circuit comprising a first N-type transistor and at least one diode, wherein a source of the first N-type transistor is coupled to said voltage input, a drain of the first N-type transistor is configured to receive a second potential, and a gate of the first N-type transistor is coupled to a predetermined bias potential that is greater than the first supply potential, and the gate also is coupled to the source of the first N-type transistor via the at least one diode, wherein the at least one diode includes a cathode coupled to the gate and an anode coupled to the source, said first N-type transistor configured to supply the first supply potential to said output buffer when said gate receives the predetermined bias potential, wherein the first supply potential is based on the second potential, and the predetermined bias potential is greater than the second potential, and

wherein said first N-type transistor has a second operating range that is greater than the first operating range of the at least one driver transistor, and wherein the first N-type transistor is configured to protect the at least one driver transistor of the output buffer at said voltage input when said second potential increases to a saturation region of the first N-type transistor, and wherein when the second potential increases to the saturation region of the first N-type transistor, the first N-type transistor limits current flowing from the drain to the source, thus providing the first supply potential at a level that is lower than a level that would damage the at least one driver transistor.

2. A circuit according to claim **1**, wherein said first transistor is a high voltage lateral N-type double-diffused metal oxide semiconductor.

3. The circuit of claim **1**, wherein the at least one driver transistor of the tri-state output buffer comprises:

the first driver transistor having a drain, a gate, and a source coupled to the source of the first N-type transistor; and

a second driver transistor having a drain coupled to the drain of the first driver transistor, a source configured to couple to a third potential, and a gate.

4. The circuit of claim **3**, wherein the tri-state output buffer further comprises:

a NAND gate having a first input configured to receive the data signal, a second input configured to receive the enable signal, and an output coupled to the gate of the first driver transistor, wherein the NAND gate is configured to NAND the data signal to produce a signal at the gate of the first driver transistor; and

a NOR gate having a first input configured to receive the data signal, a second input configured to receive an inverted enable signal, and an output coupled to the gate of the second driver transistor, wherein the NOR gate is configured to NOR the data signal and the inverted enable signal to produce a signal at the gate of the second driver transistor.

5. A circuit according to claim **3**, wherein said first driver and second driver transistors have the first operating range.

6. A circuit for buffering a data signal to a low voltage logic device, the circuit comprising:

a tri-state output buffer responsive to an enable signal and having at least one driver transistor having a first operating range, a first input configured to receive the data signal, a second input configured to receive the enable signal, a voltage input configured to receive a first supply potential, and an output configured to couple to the low voltage logic device, wherein the at least one driver transistor includes a first driver transistor coupled between the voltage input and the output, wherein the tri-state output buffer is adapted to provide a second potential at the output that corresponds to the first supply potential when the first driver transistor is on; and

a supply-input protection circuit connected to the voltage input of the tri-state buffer and configured to provide the first supply potential, the supply-input protection circuit comprising an isolation transistor, wherein a source of the isolation transistor is coupled to said voltage input, a drain of the first transistor is configured to receive a second potential, and a gate of the isolation transistor is coupled to a predetermined bias potential that is greater than the first supply potential, and the gate also is coupled to the source of the isolation transistor, said isolation transistor configured to supply the first supply potential to said output buffer when said gate receives the predetermined bias potential, wherein the first supply potential is based on the second potential, and the predetermined bias potential is greater than the second potential, and wherein said isolation transistor has a second operating range that is greater than the first operating range of the at least one driver transistor, and wherein the isolation transistor is configured to protect the at least one driver transistor of the output buffer at said voltage input when said second potential increases to a saturation region of the isolation transistor, and wherein when the second potential increases to the saturation region of the isolation transistor, the isolation transistor limits current flowing from the drain to the source, thus providing the first supply potential at a level that is lower than a level that would damage the at least one driver transistor.

7. The circuit of claim **6**, wherein the supply-input protection circuit further comprises at least one diode, wherein the at least one diode includes a cathode coupled to the gate of the isolation transistor and an anode coupled to the source of the isolation transistor.

8. The circuit of claim **6**, wherein the at least one driver transistor of the tri-state output buffer comprises:

a first driver transistor having a drain, a gate, and a source coupled to the source of the isolation transistor; and

a second driver transistor having a drain coupled to the drain of the first driver transistor, a source configured to couple to a third potential, and a gate.

9. The circuit of claim **8**, wherein the tri-state output buffer further comprises:

a NAND gate having a first input configured to receive the data signal, a second input configured to receive the enable signal, and an output coupled to the gate of the first driver transistor, wherein the NAND gate is configured to NAND the data signal to produce a signal at the gate of the first driver transistor; and

a NOR gate having a first input configured to receive the data signal, a second input configured to receive an inverted enable signal, and an output coupled to the gate of the second driver transistor, wherein the NOR gate is configured to NOR the data signal and the inverted enable signal to produce a signal at the gate of the second driver transistor.

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